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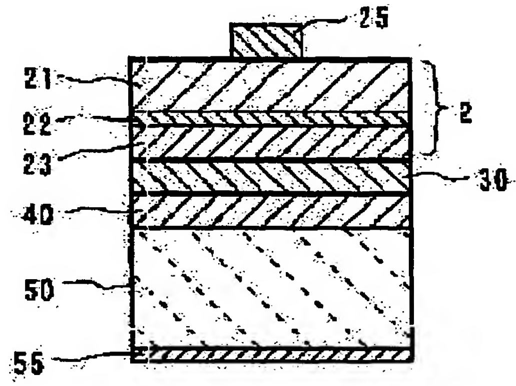
(71)Applicant : NICHIA CHEM IND LTD
(72)Inventor : NAKAMURA SHUJI

(54) NITRIDE SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF, AND LIGHT-EMITTING ELEMENT

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a nitride semiconductor device having such a structure that an electrode can be extracted mainly from the upper and lower parts, by bonding a conductive substrate to the face of a nitride semiconductor layer of a wafer which is an insulating substrate grown with the nitride semiconductor n-type layer and a p-type layer, and then removing a part or the whole part of the insulating substrate of the wafer.
SOLUTION: On the nearly entire surface of a p-type layer in the most upper layer of a nitride semiconductor layer 2, a first ohmic electrode 30 which can come into a good ohmic contact with the p-type layer is formed. On the surface of a p-type GaAs substrate 50 as a conductive substrate, a second ohmic electrode 40 which is made of Au-Zn is formed. Next, a nitride s miconductor wafer having the first ohmic electrode 30, and the p-type GaAs substrate 50 having the second ohmic electrode 40, are laminated to ach other by the ohmic electrodes and are heated to be bonded. Thereafter, the wafer bonded with the p-type GaAs substrate 50 is set in a polisher, and then a sapphire substrate 1 is lapped to remove the sapphire substrate and expose an n-type layer 21 of the nitride semiconductor layer 2.



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CLAIMS

[Claim(s)]

[Claim 1] The manufacture method of the nitride semiconductor device characterized by to have the first process which past s up a conductive substrate on the nitride semiconductor stratification plane of the wafer with which n type layer which c nsists of a nitride semiconductor, and p type layer grew, and the second process at which a part or all of the insulating substrate of the aforementioned wafer is removed, and the aforementioned n type layer is exposed after conductive substrate adhesion on an insulating substrate.

[Claim 2] the layer in which current cannot spread [the aforementioned p type layer] easily -- it is -- the aforementioned n type layer -- low -- the manufacture method of the nitride semiconductor device according to claim 1 characterized by b ing n type layer [****]

[Claim 3] The manufacture method of the claim 1 characterized by pasting up a nitride semiconductor stratification plan and a conductive substrate through an electrode or a conductive material in the first process of the above, or a nitride s miconductor device given in two.

[Claim 4] The manufacture method of the nitride semiconductor device according to claim 3 characterized by including the ohmic electrode formed in the ohmic electrode and/or the conductive substrate front face on which the aforementioned electrode was formed in the nitride semiconductor stratification plane.

[Claim 5] The manufacture method of a nitride semiconductor device according to claim 1 to 4 that the aforementioned nitride semiconductor stratification plane is characterized by being the aforementioned p type layer.

[Claim 6] A conductive substrate and the nitride semiconductor device which a nitride semiconductor comes to paste up on it and is characterized by the best layer of this nitride semiconductor being n type layer.

[Claim 7] The nitride semiconductor device according to claim 6 to which the aforementioned nitride semiconductor is characterized by having p type layer.

[Claim 8] The claim 6 to which the nitride semiconductor stratification plane which the aforementioned nitride semiconductor and the aforementioned conductive substrate paste up is characterized by being the aforementioned p type layer, or a nitride semiconductor device given in seven.

[Claim 9] The nitride semiconductor device according to claim 6 to 8 to which the aforementioned nitride semiconductor and the aforementioned conductive substrate are characterized by having pasted up through an electrode and/or a conductive material.

[Claim 10] The nitride semiconductor device according to claim 9 characterized by the aforementioned electrode containing the ohmic electrode formed in the ohmic electrode and/or the conductive substrate front face which were formed in th nitride semiconductor front face.

[Claim 11] The nitride semiconductor device according to claim 9 or 10 to which the nitride semiconductor stratification plane which pastes up the aforementioned conductive substrate is the aforementioned p type layer, and the aforementioned electrode and/or conductive material are characterized by the thing of p type layer currently mostly formed in the whole surfac .

[Claim 12] The light emitting device which is a light emitting device using the nitride semiconductor which the conductive substrate according to claim 6 to 11 pasted up, and a partial electrode is prepared in n type layer of the aforementioned b st lay r, and is characterized by the bird clapper.

[Claim 13] The light emitting device which is a light emitting device using the nitride semiconductor which the conductive substrate according to claim 9 to 11 pasted up, or a light emitting device according to claim 12, and is characterized by th ability of the aforementioned electrode and/or a conductive material to reflect the luminescence wavelength of a nitrid s miconductor.

[Translation done.]

* NOTICES *

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3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[D tailed Description of the Invention]

[0001]

[Industrial Application] this invention relates to the element which consists of a nitride semiconductor (InXAlYGa1-X-YN, 0<=X, 0<=Y, X+Y<=1) used for light-receiving devices, such as luminescence devices, such as light emitting diode and laser diode, or a photodiode.

[0002]

[Description of the Prior Art] Since a nitride semiconductor has the bandgap energy to 1.9eV - 6.0eV, it is observed as various objects for semiconductor devices, such as a light emitting device and a photo detector, and blue Light Emitting Diod using this material and the bluish green color Light Emitting Diode were just put in practical use recently.

[0003] Generally a nitride semiconductor device is obtained using vapor growths, such as MBE and MOVPE, by carrying out laminating growth of the nitride semiconductor which specified the conductivity type to n type, p type, or i type on the substrate. Although it is known that conductive substrates, such as silicon carbide besides insulating substrates, such as sapphire, a spinel, a lithium niobate, and gallium acid neodium, silicon, a zinc oxide, and gallium arsenide, can be used for a substrate The substrate which carries out grid adjustment completely with a nitride semiconductor is not yet developed, but the blue which now grew up the nitride semiconductor layer compulsorily on the sapphire with which lattice constants differ 10% or more, and the bluish green color Light Emitting Diode element are put in practical use.

[0004] Drawing 6 is the typical cross section showing the structure of the conventional blue Light Emitting Diode element. Th conventional Light Emitting Diode element has terrorism structure to the double by which the laminating of n type layer 62 and the barrier layer 63 which consist of a nitride semiconductor on silicon on sapphire 61 fundamentally, and the p typ layer 64 was carried out to order. As mentioned above, since sapphire is insulation and cannot take out an electrode from a substrate side, it considers as the so-called element of the flip chip method with which the positive electrode 65 and th negative electrode 66 were formed in the same nitride semiconductor layer front face.

[0005]

[Problem(s) to be Solved by the Invention] However, there are many troubles in the element of the conventional flip chip method which uses sapphire as a substrate. Probably, in order to take out both electrodes from the same side side in the first place, a chip size becomes large and much chips are not obtained from a wafer by it. Since the negative electrode and th positive electrode are horizontally located in a line, current flows horizontally, as a result, current density becomes high locally, and a chip generates heat [second]. Since a substrate which is called sapphire and which is very hard and does not have cl avage nature is used [third], advanced technology is needed for chip-izing. Since the cleavage plane of a nitride semiconductor which used the cleavage nature of a substrate is not made with a resonance side in case it is furthermore going to realize LD, formation of a resonance side is very difficult.

[0006] Although the attempt which grows a nitride semiconductor as mentioned above on conductive substrates, such as silicon carbide, silicon, a zinc oxide, gallium arsenide, and gallium phosphorus, is also accomplished in order to avoid the abov problems, the report of having still succeeded is not carried out.

[0007] Therefore, this invention is accomplished in view of such a situation, and the place made into the purpose is to off r th manufacture method of the nitride semiconductor device which has the structure which can take out an electrode mainly from the upper and lower sides, and a nitride semiconductor device.

[0008]

[M ans for Solving the Problem] The manufacture method of the nitride semiconductor device of this invention is characterized by to have the first process which pastes up a conductive substrate on the nitride semiconductor stratification plan of the wafer with which n type layer which consists of a nitride semiconductor, and p type layer grew, and the second proc ss at which a part or all of the insulating substrate of the aforementioned wafer is removed, and the aforementioned n type layer is exposed after conductive substrate adhesion on an insulating substrate. Moreover, with a conductive substrate, a nitrid semiconductor comes to paste up on it and the nitride semiconductor device of this invention is characterized by the b st layer of this nitride semiconductor being n type layer.

[0009] In the method of this invention, sapphire, a spinel, a lithium niobate, gallium acid neodium, etc. are used for an insulating substrate as mentioned above, and sapphire and the nitride semiconductor which grew on the spinel are preferably excellent in crystallinity. On the other hand, if it is the substrate material which has conductivity, what thing may be used, for exampl , Si, SiC, GaAs, GaP and InP, ZnSe, ZnS, ZnO, etc. can be used for the conductive substrate pasted up on a nitride semiconductor. However, a conductive substrate cannot be overemphasized by choosing the substrate of the shape of a wafer which has th almost sam c nfiguration as th insulating substrate to which th laminating of th nitride semic nductor was carried out, and has a bigger area than th further almost sam ar a or it.

[0010] On the other hand, in order to remove the insulating substrate of the wafer with which the laminating of the nitride semiconductor layer was carri d out, technology, such as polish and etching, is used. Usually, there is hundr ds of micromet rs thickness of an insulating substrat , since a nitride semiconductor layer is 20 micrometers or less even if thick, in cas polish r mov s a substrate, when it is hard to control ******, a rough portion may b removed by polish at first, a fin portion may be remov d by etching after that, and th nitride semiconductor sid needed for forming an electrode may be exposed. Moreover, when producing the element which us s an insulator as a current constriction lay r and needs it for a nitride semiconductor lay r fr nt fac , for xample like a laser lement, it is also possibl to remove nly a portion requir d

to xpose a nitride semiconductor layer by selective etching, without r moving all insulating substrat s.
[0011] Furthermore, the conductiv substrate pasted up on a nitride semiconductor layer in the method and element of this invention is characterized by having cleavage nature. GaAs, GaP, InP, SiC, etc. can be preferably used for the conductive substrate which has this cleavage nature.
[0012] Next, the method and elem nt of this invention are characterized by pasting up a nitride semiconductor stratification plane and a conductive substrate thr ugh an electrode or a conductiv material. Even if this method uses the substrat which has cleavage nature in a conductive substrate, it is applicabl similarly. Although the so-called technique of the wafer adh sion which carries out thermocompression bonding may be used f r it aft r making these mirror planes rival in the m thod of pasting up by making the adhesion sid and nitride semic nductor stratificati n plane of a conductive substrat into a mirror plane, it can paste up easily by minding an electrode or a conductiv material. If conductiv material is a nitride semiconductor and the material which can paste up a conductive substrate, what thing is sufficient as them, for exampl , they can use material, such as In, Au, a pewter, and a silver paste.
[0013] Moreover, in the aforementioned adhesion technique, it is characterized by an electrode containing the ohmic el ctrode formed in the ohmic electrode and/or the conductive substrate front face which were formed in the nitride semiconductor layer front face. In addition, with an ohmic electrode, it is defined as an ohmic electrode on these specifications including metals, such as the metal for thick adhesion of the thickness attached on the thin ohmic electrode and lectrode of the thickness generally formed in a nitride semiconductor front face, for example, Au, In, aluminum, tc. As an ohmic electrode material formed in a nitride semiconductor layer front face, if n type layer is an adhesion side, a kind of mat rial of aluminum, Cr(s), Ti, and In(s) which were shown in JP,5-291621,A, the electrode which made Ti especially the side which touches n type layer preferably, and the material containing Ti-aluminum shown in JP,7-45867,A can be mentioned at least. Moreover, if an adhesion side is p type layer, a kind of material of Au(s), Pt(s), Ag, and nickel which wer similarly shown in JP,5-291621,A, and the electrode which made nickel especially the side which touches p type layer pr ferably can be mentioned at least.
[0014] A nitride semiconductor is performed, in order for p type layer to be hard to be obtained and to obtain p type lay r, for xample, after electron beam irradiation which is indicated by JP,3-218625,A, and thermal annealing processing which is indicated by JP,5-183189,A growing, and p type layer on the front face of the maximum is formed into low resistance. For this reason, as for the nitride semiconductor wafer, the best layer is p type layer in many cases. Then, in case this nitrid s miconductor wafer and a conductive substrate are pasted up, especially the thing for which a conductive p type substrate is pasted up through the ohmic electrode formed in p type layer is desirable.
[0015] On the other hand, if for example, a conductive substrate is n type GaAs as an ohmic electrode already formed in th conductive substrate of one of the two's adhesion side, Ag-Sn, In-Sn, nickel-Sn, Au-Sn, Au-Si, Au-germanium, etc. can b us d, and if it is p type GaAs, Au-Zn, Ag-Zn, Ag-In, etc. can be used. In addition, although an ohmic electrode material w ll-known also about SiC and Si can be used, especially the thing for which a conductive p type substrate is pasted up through the ohmic electrode of the conductive substrate as mentioned above is desirable.
[0016]
[Function] With the method and element of this invention, the conductive substrate is pasted up on the nitride s miconductor layer. That is, although the various elements from which a nitride semiconductor is obtained from a nitride s miconductor with the wafer which grew on the insulating substrate cannot but serve as flip chip form, they serve as a substrate in which a conductive substrate forms an electrode by pasting up a conductive substrate on the nitride semiconductor layer of the wafer best layer. Then, since a nitride semiconductor layer will be exposed if an insulating substrate is removed, another electrode can be formed in the exposed nitride semiconductor stratification plane, and not th element with which an electrode like before was horizontally located in a line but the element which the mutual electrode countered can be produced.
[0017] Next, if the material which has cleavage nature in the conductive substrate to paste up is chosen, the nitride s miconductor which grew on the insulating substrate without cleavage nature can also divide in the shape of a chip using th cleavage nature of the pasted-up conductive substrate. For this reason, the small element of a chip size becomes is easy to be obtained, and the laser element which makes the cleavage plane of a nitride semiconductor an optical resonanc side further can be produced now.
[0018] moreover, although there is also the method of a nitride semiconductor stratification plane and a conductive substrate b ing the technology generally called wafer adhesion, and pasting up, it is desirable in order to also stabilize the electrical prop rty between a conductive substrate and a nitride semiconductor layer, if it pastes up through the electrode of a nitride semiconductor layer, the electrode of a conductive substrate, or a conductive material especially When choosing the material which can furthermore reflect the luminescence wavelength of nitride semiconductors, such as Au, aluminum, and Ag, as this conductive material and a light emitting device is produced, the light which comes to the conductive substrate which such conductive material pasted up is reflected, and since there is an operation returned to a nitride semiconductor layer sid , the luminous efficiency of a light emitting device improves.
[0019] If the ohmic electrode formed in the ohmic electrode and/or the conductive substrate front face which were formed in the nitride semiconductor layer front face especially as a charge of a binder is included, when a luminescence devic lik a light mitting device will be produced, for example, resistance becomes low and there is an operation which reduces Vf of a d vice.
[0020]
[Exampl] Hereafter, this invention is xplained in full detail in the example. Drawing 1 or drawing 3 is a waf r explaining on process f th m thod of this invention, and th typical cross section of a conductiv substrate, and drawing 4 is th typical cr ss section showing the structure of the nitride semiconductor light emitting devic obtained according to th exampl 1, and describes an xample 1 b low bas d n th se drawings.
[0021] Th nitride semiconductor lay r 2 prepar s f r the front face f [xampl 1] silicon n sapphir 1 the wafer by which the laminating was carri d out. In additi n, the nitride semiconductor layer 2 has terrorism structure to the double which has at l ast n type layer 21 which consists of AlXGa1-XN (0<=X<=1) by which the donor impurity was dop d sequ ntially from silic n on sapphire 1, the barri r layer 22 which consists of InYGa1-YN (0< Y<1), and p typ layer 23 which consists of AlXGa1-XN (0<=X<=1) by which accept r impurity was doped. In addition, p typ layer 23 of the b st layer is f rm d into low

resistance by annealing 400 degrees C or more.

[0022] Next, as shown in drawing 1 , the ohmic electrode 30 of th front face f th nitride s miconductor lay r 2 which contains nickel and Au on the whole surface is mostly formed by 500A thickness. That is, the first ohmic lectrode 30 from which as desirable on the whole surface OMIKKU of p type lay r of the best layer of the nitride semiconduct r layer 2 as p type layer is obtained mostly is formed. in order are furthermore alike on the ohmic electrode 30 and to improve an adh siv property, 0.1 micrometers of Au thin films are formed

[0023] The p type GaAs substrate 50 which, on the other hand, has the almost same size as silicon on sapphir 1 as a conductive substrate is prepared, and the second ohmic electrode 40 which c nsists of Au-Zn is formed in the front face of this p type GaAs substrate 50 by 500A thickness. In order to improve an adhesive property on the second ohmic lectrode 40 furthermore, 0.1 micromet rs of Au thin films are formed.

[0024] Next, the ohmic electrodes of the nitride semiconductor wafer which has the first ohmic electrode 30 as shown in drawing 2 , and the p type GaAs substrate 50 which has the second ohmic electrode 40 are stuck by pressure by lamination and heating. However, it is made to become parallel [the silicon on sapphire 1 of a wafer, and the p type GaAs substrat 50] at the time of sticking by pressure. It is because the level surface of the nitride semiconductor layer exposed does not come out in the process which removes the following silicon on sapphire unless it is parallel. Moreover, although Au was used in order to paste up the first ohmic electrode 30 and the second ohmic electrode 40, it is also possible to paste up through conductive material, such as an indium, tin, a pewter, and a silver paste, among electrodes 30 and 40. In addition, in case the p type GaAs substrate 50 is pasted up, doubling the direction of a cleavage with a substrate 50 with the cleavage nature of a nitride semiconductor layer, and having pasted up cannot be overemphasized.

[0025] Next, the wafer on which the p type GaAs substrate 50 was pasted up is installed in the burnisher, silicon on sapphir 1 is wrapped, silicon on sapphire is removed, and n type layer 21 of the nitride semiconductor layer 2 is exposed. In addition, after wrapping silicon on sapphire 1 so that the thickness of about several micrometers may remain, it is [in / this process] also possible to remove the silicon on sapphire which remained further by etching. The structure of the wafer after silicon-on-sapphire 1 removal is shown in drawing 3 .

[0026] n type layer after polishing the front face of n type layer 21 exposed at the end — ohmic one — the negative el ctrode 25 which consists of Ti-aluminum as an electrode of business is formed, and the positive electrode 55 which consists of Au-Zn as an ohmic electrode as well as the p type GaAs substrate 50 on the other hand is formed in the whole surface

[0027] The wafer with which the positive electrode and the negative electrode were formed as mentioned above is divid d into the luminescence chip of 200-micrometer angle using the cleavage nature of a p type GaAs substrate. The typical cross section showing the structure of the luminescence chip after separation is shown in drawing 4 . By energizing between an el ctrode 25 and 55, this luminescence chip shows the structure of a Light Emitting Diode element where a barrier layer 22 emits light. Since it was reflected by the interface of the first ohmic electrode 30 and p type layer 23 and, as for this light emitting device, luminescence of a barrier layer 22 was not absorbed by the p type GaAs substrate 50, compared with the conventional light emitting device, the radiant power output increased 50% or more.

[0028] Moreover, although sapphire and the conductive substrate explained p type GaAs, they may use an insulating substrate like a spinel and neodium gallate described above besides sapphire to the insulating substrate, for example, and as for this example, an insulating substrate may use a substrate like Si and ZnO for a conductive substrate.

[0029] In case silicon on sapphire 1 is wrapped in the [example 2] example 1, it wraps so that it may remain by the thickness whose silicon on sapphire 1 is 5 micrometers. Next, the mask of the configuration which can form a current constriction layer in th front face of the silicon on sapphire 1 which remained is formed, etching removes the silicon on sapphire 1 of mask opening by the etching system, and a part of n type layer 21 is exposed. A positive electrode 55 is formed in n type lay r lik th exposure back at a negative electrode 25 and the p type GaAs substrate 50.

[0030] Next, using the cleavage nature of the p type GaAs substrate 50, it dissociates in the shape of a chip, and considers as a laser element. Drawing 5 is the typical cross section showing the structure of the laser element, and the silicon on sapphire 1 which it left intentionally is acting as a current constriction layer of a laser element. Although this example showed the example which leaves silicon on sapphire as a current constriction layer, in addition after it all removes silicon on sapphire 1 like an example 1 to form the current constriction layer of a laser element, you may form it on the nitride s miconductor layer which exposed an insulator layer like SiO_2 and TiO_2, for example.

[0031]

[Effect of the Invention] Since the nitride semiconductor device which has a conductive substrate is realizable according to th m thod of this invention as explained above, the small element of a chip size can be offered. Moreover, since the electrodes formed in the element have countered, current flows uniformly in a nitride semiconductor layer, calorific value b com s small and it also becomes possible to realize a laser element. The cleavage of a nitride semiconductor becom s possible still more easily, and since the cleavage plane is made with a resonator, production of a laser element becomes asy. If a luminescence device is realized further again, since luminescence of a nitride semiconductor layer will be reflected on an lectrode front face by the electrode which pasted up the nitride semiconductor layer and the conductive substrate, a radiant power output can also be increased.

[0032] As the conventional nitride semiconductor Light Emitting Diode was shown in drawing 6 , the positive electrode 65 of the front face of p type layer 64 which penetrates light was mostly formed in the whole surface. This is because the current of p type layer cannot spread easily. 50% or more of the light which emits light by this positive electrode 65 was absorbed. how ver, according to the element of this inv ntion, it is shown in drawing 4 and drawing 5 — as — l w — since n type lay r [****] 21 turns into the b st layer, it becomes unnecessary to pr pare a whole surfac el ctrode like b fore, and is good at a small partial l ctrod Th refore, the jection fficiency of th light from a nitrid semiconductor layer sid improves by l aps and bounds, and a radiant pow r utput improves. Thus, wh n this inv ntion realizes the devic which used the nitride s miconductor, the utility valu n industry is v ry large.

[Translation don .]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The type section view of the nitride semiconductor wafer explaining one process of the method of this invention.
[Drawing 2] The type section view of the nitride semiconductor wafer explaining one process of the method of this invention.
[Drawing 3] The type section view of the nitride semiconductor wafer explaining one process of the method of this invention.
[Drawing 4] The type section view showing the structure of the nitride semiconductor device concerning one example of this invention.
[Drawing 5] The type section view showing the structure of the nitride semiconductor device concerning other examples of this invention.
[Drawing 6] The type section view showing the structure of the conventional nitride semiconductor light emitting device.
[Description of Notations]
1 .... Silicon on sapphire
2 .... Nitride semiconductor layer
21 .... n type layer
22 .... Barrier layer
23 .... p type layer
30 .... First ohmic electrode
40 .... Second ohmic electrode
50 .... p type GaAs substrate
25 .... Negative electrode
55 .... Positive electrode

[Translation done.]

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(71) 出願人　000226057
日亜化学工業株式会社
徳島県阿南市上中町岡491番地100

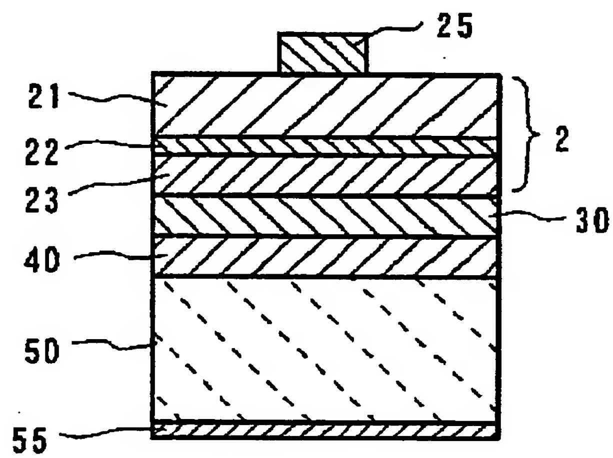
(72) 発明者　中村　修二
徳島県阿南市上中町岡491番地100　日亜化学工業株式会社内

(54)【発明の名称】窒化物半導体素子の製造方法及び窒化物半導体素子、並びに発光素子

(57)【要約】

【目的】　上下より電極を取り出せる構造を有する窒化物半導体素子の製造方法、および窒化物半導体素子を提供する。

【構成】　絶縁性基板の上に窒化物半導体層が成長されたウェーハの窒化物半導体層面に導電性基板を接着する第一の工程と、導電性基板接着後、前記ウェーハの絶縁性基板の一部、又は全部を除去して窒化物半導体層を露出させる第二の工程とを備え、露出させた窒化物半導体層と、導電性基板とに対向する電極を設ける。



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【特許請求の範囲】

【請求項１】絶縁性基板の上に、窒化物半導体からなるｎ型層と、ｐ型層とが成長されたウェーハの窒化物半導体層面に、導電性基板を接着する第一の工程と、導電性基板接着後、前記ウェーハの絶縁性基板の一部、又は全部を除去して前記ｎ型層を露出させる第二の工程とを備えることを特徴とする窒化物半導体素子の製造方法。

【請求項２】前記ｐ型層が電流の広がりにくい層であって、前記ｎ型層が低抵抗なｎ型層であることを特徴とする請求項１記載の窒化物半導体素子の製造方法。

【請求項３】前記第一の工程において、窒化物半導体層面と導電性基板とを電極、又は導電性材料を介して接着することを特徴とする請求項１、又は２記載の窒化物半導体素子の製造方法。

【請求項４】前記電極が窒化物半導体層面に形成されたオーミック電極及び／又は導電性基板表面に形成されたオーミック電極を含むことを特徴とする請求項３記載の窒化物半導体素子の製造方法。

【請求項５】前記窒化物半導体層面が、前記ｐ型層であることを特徴とする請求項１乃至４記載の窒化物半導体素子の製造方法。

【請求項６】導電性基板と、その上に窒化物半導体とが接着されてなり、該窒化物半導体の最上層がｎ型層であることを特徴とする窒化物半導体素子。

【請求項７】前記窒化物半導体が、ｐ型層を有することを特徴とする請求項６記載の窒化物半導体素子。

【請求項８】前記窒化物半導体と前記導電性基板とが接着される窒化物半導体層面が、前記ｐ型層であることを特徴とする請求項６、又は７記載の窒化物半導体素子。

【請求項９】前記窒化物半導体と前記導電性基板とが、電極及び／又は導電性材料を介して接着されていることを特徴とする請求項６乃至８記載の窒化物半導体素子。

【請求項１０】前記電極が、窒化物半導体表面に形成されたオーミック電極及び／又は導電性基板表面に形成されたオーミック電極を含むことを特徴とする請求項９記載の窒化物半導体素子。

【請求項１１】前記導電性基板を接着する窒化物半導体層面が、前記ｐ型層であり、前記電極及び／又は導電性材料が、ｐ型層のほぼ全面に形成されていることを特徴とする請求項９又は１０記載の窒化物半導体素子。

【請求項１２】請求項６乃至１１に記載の導電性基板が接着された窒化物半導体を用いた発光素子であって、前記最上層のｎ型層に、部分電極が設けられてなることを特徴とする発光素子。

【請求項１３】請求項９乃至１１に記載の導電性基板が接着された窒化物半導体を用いた発光素子、若しくは請求項１２記載の発光素子であって、前記電極及び／又は導電性材料が、窒化物半導体の発光波長を反射できることを特徴とする発光素子。

【発明の詳細な説明】

2

【０００１】

【産業上の利用分野】本発明は発光ダイオード、レーザダイオード等の発光デバイス、又はフォトダイオード等の受光デバイスに使用される窒化物半導体（$In_XAl_YGa_{1-X-Y}N$、$0 \leq X$、$0 \leq Y$、$X+Y \leq 1$）よりなる素子に関する。

【０００２】

【従来の技術】窒化物半導体はそのバンドギャップエネルギーが１．９ｅＶ～６．０ｅＶまであるので発光素子、受光素子等の各種半導体デバイス用として注目されており、最近この材料を用いた青色ＬＥＤ、青緑色ＬＥＤが実用化されたばかりである。

【０００３】一般に窒化物半導体素子はＭＢＥ、ＭＯＶＰＥ等の気相成長法を用いて、基板上にｎ型、ｐ型あるいはｉ型等に導電型を規定した窒化物半導体を積層成長させることによって得られる。基板には例えばサファイア、スピネル、ニオブ酸リチウム、ガリウム酸ネオジウム等の絶縁性基板の他、炭化ケイ素、シリコン、酸化亜鉛、ガリウム砒素等の導電性基板が使用できることが知られているが、窒化物半導体と完全に格子整合する基板は未だ開発されておらず、現在のところ、格子定数が１０％以上も異なるサファイアの上に窒化物半導体層を強制的に成長させた青色、青緑色ＬＥＤ素子が実用化されている。

【０００４】図６は従来の青色ＬＥＤ素子の構造を示す模式的な断面図である。従来のＬＥＤ素子は、基本的にサファイア基板６１の上に窒化物半導体よりなるｎ型層６２と活性層６３とｐ型層６４とが順に積層されたダブルヘテロ構造を有している。前記のようにサファイアは絶縁性であり基板側から電極を取り出すことができないので、同一窒化物半導体層表面に正電極６５と負電極６６とが設けられた、いわゆるフリップチップ方式の素子とされている。

【０００５】

【発明が解決しようとする課題】しかしながら、サファイアを基板とする従来のフリップチップ方式の素子には数々の問題点がある。まず第一に、同一面側から両方の電極を取り出すためチップサイズが大きくなり多数のチップがウェーハから得られない。第二に、負電極と正電極とが水平方向に並んでいるため電流が水平方向に流れ、その結果電流密度が局部的に高くなりチップが発熱する。第三にサファイアという非常に硬く、劈開性のない基板を使用しているので、チップ化するのに高度な技術を必要とする。さらにＬＤを実現しようとする際には基板の劈開性を用いた窒化物半導体の劈開面を共振面とできないので共振面の形成が非常に困難である。

【０００６】以上のような問題を回避するため、上記のように炭化ケイ素、シリコン、酸化亜鉛、ガリウム砒素、ガリウムリン等の導電性基板の上に窒化物半導体を成長する試みも成されているが、未だ成功したという報

告はされていない。

【０００７】従って本発明はこのような事情を鑑み成されたものであって、その目的とするところは、主として上下より電極を取り出せる構造を有する窒化物半導体素子の製造方法、および窒化物半導体素子を提供することにある。

【０００８】

【課題を解決するための手段】本発明の窒化物半導体素子の製造方法は、絶縁性基板の上に、窒化物半導体からなるｎ型層と、ｐ型層とが成長されたウェーハの窒化物半導体層面に導電性基板を接着する第一の工程と、導電性基板接着後、前記ウェーハの絶縁性基板の一部、又は全部を除去して前記ｎ型層を露出させる第二の工程とを備えることを特徴とする。また、本発明の窒化物半導体素子は導電性基板と、その上に窒化物半導体とが接着されてなり、該窒化物半導体の最上層がｎ型層であることを特徴とする。

【０００９】本発明の方法において、絶縁性基板には前記のようにサファイア、スピネル、ニオブ酸リチウム、ガリウム酸ネオジウム等が用いられ、好ましくはサファイア、スピネルの上に成長された窒化物半導体が結晶性に優れている。一方、窒化物半導体に接着する導電性基板には、導電性を有する基板材料であればどのようなものでも良く、例えばＳｉ、ＳｉＣ、ＧａＡｓ、ＧａＰ、ＩｎＰ、ＺｎＳｅ、ＺｎＳ、ＺｎＯ等を用いることができる。但し、導電性基板は窒化物半導体が積層された絶縁性基板とほぼ同じ形状を有し、さらにほぼ同じ面積か、あるいはそれよりも大きな面積を有するウェーハ状の基板を選択することはいうまでもない。

【００１０】一方、窒化物半導体層が積層されたウェーハの絶縁性基板を除去するには、例えば研磨、エッチング等の技術を用いる。通常絶縁性基板の厚さは数百μｍあり、窒化物半導体層は厚くても２０μｍ以下であるので、研磨により基板を除去する際に研磨厚が制御しにくい場合は、最初研磨で大まかな部分を除去し、その後エッチングで細かい部分を除去して、電極を形成するのに必要とする窒化物半導体面を露出させても良い。また例えばレーザ素子のように絶縁物を電流狭窄層として窒化物半導体層表面に必要とする素子を作製する場合には、絶縁性基板全てを除去せずに、選択エッチングにより窒化物半導体層を露出させるのに必要な部分のみを除去することも可能である。

【００１１】さらに本発明の方法及び素子において、窒化物半導体層に接着する導電性基板は劈開性を有することを特徴とする。この劈開性を有する導電性基板には、例えばＧａＡｓ、ＧａＰ、ＩｎＰ、ＳｉＣ等を好ましく用いることができる。

【００１２】次に本発明の方法及び素子は窒化物半導体層面と導電性基板とを電極、又は導電性材料を介して接着することを特徴とする。この方法は導電性基板に劈開性のある基板を使用しても同様に適用可能である。接着する方法には、導電性基板の接着面と、窒化物半導体層面とを鏡面として、それら鏡面同士を張り合わせた後、熱圧着するいわゆるウェーハ接着の手法を用いてもよいが、電極又は導電性材料を介することにより簡単に接着することができる。導電性材料は窒化物半導体と導電性基板を接着できる材料であればどのようなものでも良く、例えばＩｎ、Ａｕ、ハンダ、銀ペースト等の材料を使用することができる。

【００１３】また前記接着手法において、電極は窒化物半導体層表面に形成されたオーミック電極及び／又は導電性基板表面に形成されたオーミック電極を含むことを特徴とする。なお、オーミック電極とは、一般に窒化物半導体表面に形成される膜厚の薄いオーミック電極と、その電極の上に付けられた膜厚の厚い接着用の金属、例えばＡｕ、Ｉｎ、Ａｌ等の金属を含んで本明細書ではオーミック電極と定義する。窒化物半導体層表面に形成するオーミック電極材料としては、ｎ型層が接着面であれば例えば特開平５－２９１６２１号公報に示されたＡｌ、Ｃｒ、Ｔｉ、Ｉｎの内の少なくとも一種の材料、特に好ましくはＴｉをｎ型層と接する側とした電極、また特開平７－４５８６７号公報に示されたＴｉ－Ａｌを含む材料を挙げることができる。また接着面がｐ型層であれば同じく特開平５－２９１６２１号公報に示されたＡｕ、Ｐｔ、Ａｇ、Ｎｉの内の少なくとも一種の材料、特に好ましくはＮｉをｐ型層と接する側とした電極を挙げることができる。

【００１４】窒化物半導体はｐ型層が得られにくく、ｐ型層を得るため例えば特開平３－２１８６２５号公報に開示されるような電子線照射、また特開平５－１８３１８９号公報に開示されるような熱的アニーリング処理が成長後に行われ、最表面のｐ型層が低抵抗化される。このため窒化物半導体ウェーハは最上層がｐ型層になっていることが多い。そこで、この窒化物半導体ウェーハと導電性基板を接着する際には、ｐ型層に形成されたオーミック電極を介してｐ型の導電性基板とを接着することが特に望ましい。

【００１５】一方、もう片方の接着面の導電性基板に形成するオーミック電極としては例えば導電性基板がｎ型ＧａＡｓであれば、Ａｇ－Ｓｎ、Ｉｎ－Ｓｎ、Ｎｉ－Ｓｎ、Ａｕ－Ｓｎ、Ａｕ－Ｓｉ、Ａｕ－Ｇｅ等を用いることができ、ｐ型ＧａＡｓであれば、Ａｕ－Ｚｎ、Ａｇ－Ｚｎ、Ａｇ－Ｉｎ等を用いることができる。その他ＳｉＣ、Ｓｉ等についても公知のオーミック電極材料を用いることができるが前記のようにｐ型の導電性基板をその導電性基板のオーミック電極を介して接着することが特に望ましい。

【００１６】

【作用】本発明の方法及び素子では窒化物半導体層に導電性基板を接着している。つまり、窒化物半導体が絶縁

性基板の上に成長されたウェーハでは、窒化物半導体より得られる各種素子はフリップチップ形式とならざるを得ないが、導電性基板をウェーハ最上層の窒化物半導体層に接着することにより、導電性基板が電極を形成する基板となる。その後、絶縁性基板を除去すると窒化物半導体層が露出するので、露出した窒化物半導体層面にもう一方の電極を形成することができ、従来のような電極が水平方向に並んだ素子ではなく、互いの電極が対向した素子を作製することができる。

【００１７】次に接着する導電性基板に劈開性のある材料を選択すると、劈開性のない絶縁性基板の上に成長された窒化物半導体でも、接着された導電性基板の劈開性を利用してチップ状に分割できる。このためチップサイズの小さい素子が得られやすくなり、さらに窒化物半導体の劈開面を光共振面とするレーザ素子が作製できるようになる。

【００１８】また窒化物半導体層面と導電性基板とは一般にウェーハ接着と呼ばれる技術で接着する方法もあるが、特に窒化物半導体層の電極、若しくは導電性基板の電極、又は導電性材料を介して接着すると導電性基板と窒化物半導体層との間の電気的特性も安定化するため好ましい。さらにこの導電性材料としてＡｕ、Ａｌ、Ａｇ等の窒化物半導体の発光波長を反射できる材料を選択すれば、発光素子を作製した際、これらの導電性材料が接着した導電性基板に来る光を反射して、窒化物半導体層の側に戻す作用があるので発光素子の発光効率が向上する。

【００１９】特に接着材料として、窒化物半導体層表面に形成されたオーミック電極及び／又は導電性基板表面に形成されたオーミック電極を含めば、例えば発光素子のような発光デバイスを作製すると、抵抗値が低くなりデバイスのＶｆを低下させる作用がある。

【００２０】

【実施例】以下、実施例で本発明を詳説する。図１乃至図３は本発明の方法の一工程を説明するウェーハ及び導電性基板の模式的な断面図であり、図４は実施例１により得られた窒化物半導体発光素子の構造を示す模式的な断面図であり、以下これらの図を元に実施例１を述べる。

【００２１】［実施例１］サファイア基板１の表面に窒化物半導体層２が積層されたウェーハを用意する。なお窒化物半導体層２はサファイア基板１から順にドナー不純物がドープされた$Al_XGa_{1-X}N$（$0 \leqq X \leqq 1$）よりなるｎ型層２１と、$In_YGa_{1-Y}N$（$0 < Y < 1$）よりなる活性層２２と、アクセプター不純物がドープされた$Al_XGa_{1-X}N$（$0 \leqq X \leqq 1$）よりなるｐ型層２３とを少なくとも有するダブルヘテロ構造を有している。なお最上層のｐ型層２３は４００℃以上のアニーリングにより低抵抗化されている。

【００２２】次に図１に示すように窒化物半導体層２の表面のほぼ全面にＮｉとＡｕを含むオーミック電極３０を５００オングストロームの膜厚で形成する。つまり窒化物半導体層２の最上層のｐ型層のほぼ全面にｐ型層と好ましいオーミックが得られる第一のオーミック電極３０を形成する。さらにそのオーミック電極３０の上にに接着性を良くするためにＡｕ薄膜を０．１μｍ形成する。

【００２３】一方、導電性基板として、サファイア基板１とほぼ同じ大きさを有するｐ型ＧａＡｓ基板５０を用意し、このｐ型ＧａＡｓ基板５０の表面にＡｕ－Ｚｎよりなる第二のオーミック電極４０を５００オングストロームの膜厚で形成する。さらにその第二のオーミック電極４０の上に接着性を良くするためにＡｕ薄膜を０．１μｍ形成する。

【００２４】次に、図２に示すように第一のオーミック電極３０を有する窒化物半導体ウェーハと、第二のオーミック電極４０を有するｐ型ＧａＡｓ基板５０とのオーミック電極同士を貼り合わせ、加熱により圧着する。但し、圧着時ウェーハのサファイア基板１とｐ型ＧａＡｓ基板５０とは平行となるようにする。平行でないと次のサファイア基板を除去する工程において、露出される窒化物半導体層の水平面が出ないからである。また第一のオーミック電極３０と第二のオーミック電極４０とを接着するためにＡｕを使用したが、この他電極３０と４０との間にインジウム、錫、ハンダ、銀ペースト等の導電性材料を介して接着することも可能である。なおｐ型ＧａＡｓ基板５０を接着する際に窒化物半導体層の劈開性と、基板５０との劈開方向を合わせて接着してあることは言うまでもない。

【００２５】次にｐ型ＧａＡｓ基板５０を接着したウェーハを研磨器に設置し、サファイア基板１のラッピングを行い、サファイア基板を除去して、窒化物半導体層２のｎ型層２１を露出させる。なおこの工程において、例えばサファイア基板１を数μｍ程度の厚さが残るようにラッピングした後、さらに残ったサファイア基板をエッチングにより除去することも可能である。サファイア基板１除去後のウェーハの構造を図３に示す。

【００２６】最後に露出したｎ型層２１の表面をポリシングした後、ｎ型層にオーミック用の電極としてＴｉ－Ａｌよりなる負電極２５を形成し、一方ｐ型ＧａＡｓ基板５０には同じくオーミック電極としてＡｕ－Ｚｎよりなる正電極５５を全面に形成する。

【００２７】以上のようにして正電極および負電極が形成されたウェーハを、ｐ型ＧａＡｓ基板の劈開性を利用して２００μｍ角の発光チップに分離する。分離後の発光チップの構造を示す模式的な断面図を図４に示す。この発光チップは電極２５と５５間に通電することにより、活性層２２が発光するＬＥＤ素子の構造を示している。この発光素子は活性層２２の発光が第一のオーミック電極３０とｐ型層２３との界面で反射され、ｐ型Ｇａ

Ａｓ基板５０に吸収されることがないので、従来の発光素子に比べて発光出力が５０％以上増大した。

【００２８】またこの例は絶縁性基板がサファイア、導電性基板がｐ型ＧａＡｓについて説明したが、絶縁性基板にはサファイアの他に例えば前記したスピネル、ネオジウムガレートのような絶縁性基板を用いても良く、また導電性基板にはＳｉ、ＺｎＯのような基板を用いても良い。

【００２９】［実施例２］実施例１においてサファイア基板１をラッピングする際、サファイア基板１が５μｍの膜厚で残るようにラッピングする。次に残ったサファイア基板１の表面に電流狭窄層が形成できるような形状のマスクを形成し、エッチング装置でマスク開口部のサファイア基板１をエッチングにより除去し、ｎ型層２１の一部を露出させる。露出後同様にしてｎ型層に負電極２５とｐ型ＧａＡｓ基板５０に正電極５５を形成する。

【００３０】次にｐ型ＧａＡｓ基板５０の劈開性を用いて、チップ状に分離してレーザ素子とする。図５はそのレーザ素子の構造を示す模式的な断面図であり、故意に残したサファイア基板１がレーザ素子の電流狭窄層として作用している。この例は電流狭窄層としてサファイア基板を残す例を示したが、この他にレーザ素子の電流狭窄層を形成するには実施例１のようにサファイア基板１を全部除去してから、例えばSiO_2、TiO_2のような絶縁膜を露出した窒化物半導体層の上に形成しても良い。

【００３１】

【発明の効果】以上説明したように、本発明の方法によると導電性基板を有する窒化物半導体素子が実現できるので、チップサイズの小さい素子を提供することができる。また素子に形成した電極同士が対向しているので、電流が窒化物半導体層に均一に流れ発熱量が小さくなり、レーザ素子を実現することも可能となる。さらに容易に窒化物半導体の劈開が可能となり、その劈開面を共振器とできるためレーザ素子の作製が容易となる。さらにまた発光デバイスを実現すると、窒化物半導体層と導電性基板とを接着した電極により、窒化物半導体層の発光が電極表面で反射されるので発光出力も増大させることができる。

【００３２】従来の窒化物半導体ＬＥＤは図６に示すようにｐ型層６４の表面のほぼ全面に光を透過する正電極６５が形成されていた。これはｐ型層の電流が広がりにくいことによる。この正電極６５により発光する光の５０％以上が吸収されていた。しかし本発明の素子によると図４および図５に示すように低抵抗なｎ型層２１が最上層となるので、従来のように全面電極を設ける必要がなくなり、小さな部分電極でよい。従って窒化物半導体層側からの光の取り出し効率が飛躍的に向上し発光出力が向上する。このように本発明は窒化物半導体を用いたデバイスを実現する上で産業上の利用価値は非常に大きい。

【図面の簡単な説明】

【図１】　本発明の方法の一工程を説明する窒化物半導体ウェーハの模式断面図。

【図２】　本発明の方法の一工程を説明する窒化物半導体ウェーハの模式断面図。

【図３】　本発明の方法の一工程を説明する窒化物半導体ウェーハの模式断面図。

【図４】　本発明の一実施例に係る窒化物半導体素子の構造を示す模式断面図。

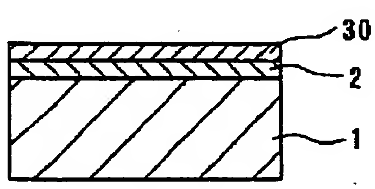
【図５】　本発明の他の実施例に係る窒化物半導体素子の構造を示す模式断面図。

【図６】　従来の窒化物半導体発光素子の構造を示す模式断面図。

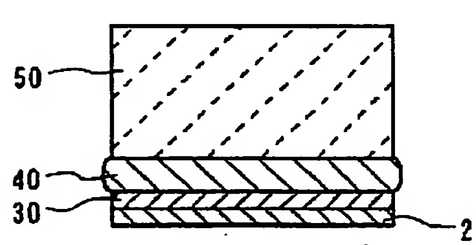
【符号の説明】

１・・・・サファイア基板
２・・・・窒化物半導体層
２１・・・・ｎ型層
２２・・・・活性層
２３・・・・ｐ型層
３０・・・・第一のオーミック電極
４０・・・・第二のオーミック電極
５０・・・・ｐ型ＧａＡｓ基板
２５・・・・負電極
５５・・・・正電極

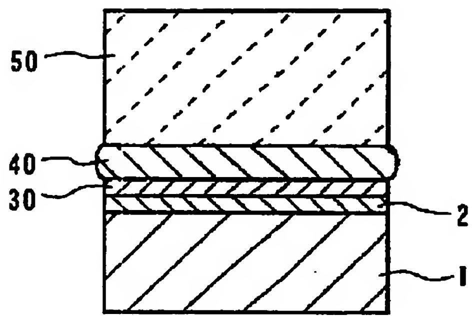
【図１】



【図３】



【図２】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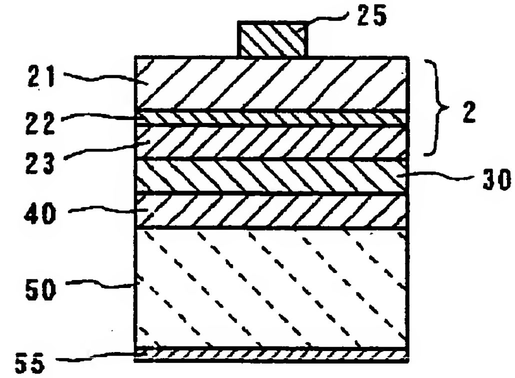
40
30
2
1

【図４】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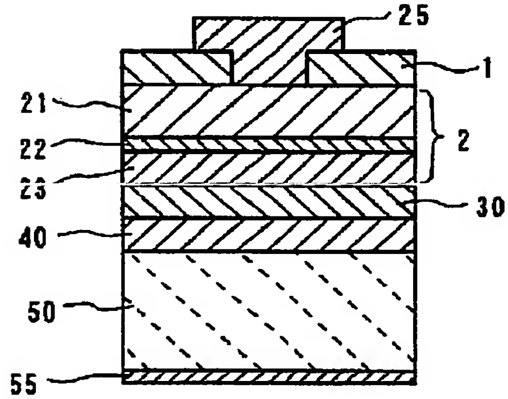
21
22
23
2
30
40
50
55

【図５】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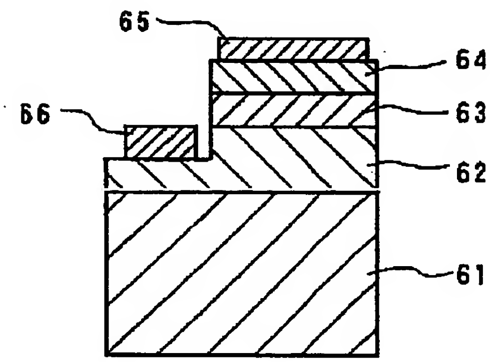
21
22
23
2
30
40
50
55

【図６】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61